Amendments to the Claims:

This listing of claims replaces all prior versions and listings:

1. (Currently amended) Apparatus for generating a clock signal comprising:

an oscillator circuit having an inverting amplifier and a resonator ~~configured~~ to generate an oscillating signal; and

a bias circuit having a relatively constant current source ~~configured~~ to create a relatively constant bias voltage to bias the inverting amplifier in an operating state that can sustain the oscillating signal, the current source and the inverting amplifier not forming a feedback loop.

2. (Original) The apparatus of claim 1 wherein the inverting amplifier has an input terminal and an output terminal coupled to a first terminal and a second terminal of the resonator, respectively.

3. (Original) The apparatus of claim 1 wherein the inverting amplifier comprises a plurality of MOSFETs that operate in the sub-threshold region when the inverting amplifier and the relatively constant current source reach an operation state capable of sustaining oscillation of the oscillator circuit.

4. (Original) The apparatus of claim 1 wherein the bias circuit comprises a plurality of MOSFETs that operate in the sub-threshold region when the inverting amplifier and the bias circuit reach an operation state capable of sustaining the oscillation of the oscillator circuit.

5. (Currently amended) The apparatus of claim 1, wherein the relatively constant current source has a first leg and a second leg, the first leg ~~configured~~ to receive a first current flowing therethrough, the second leg ~~configured~~ to receive a second current flowing

therethrough, the first current being in a substantially fixed ratio to the second current, the first leg providing the bias voltage on a node electrically connected to a node of the inverting amplifier, the bias voltage being in a predefined relationship with the current flowing through the first leg.

6. (Previously presented) The apparatus of claim 5 wherein the second-leg has a component for providing a negative feedback in response to a change in the amount of current flowing through the second leg.

7. (Original) The apparatus of claim 1 wherein the bias circuit includes a bias node, and the relatively constant current source is configured to create the bias voltage at the bias node.

8. (Original) The apparatus of claim 7 wherein the bias circuit is disposed within an integrated circuit package and connected to the amplifier only through the bias node.

9. (Original) The apparatus of claim 8 wherein the bias circuit and the amplifier are disposed within the same integrated circuit package.

10. (Currently amended) The apparatus of claim 1, further comprising an excitation circuit ~~configured~~ to provide an excitation to enable the bias circuit to start operation and to provide a stable bias voltage.

11. (Currently amended) The apparatus of claim 10, further comprising an inhibit circuit ~~configured~~ to inhibit the excitation when the bias circuit is capable of sustaining the bias voltage at a predetermined level.

12. (Original) The apparatus of claim 1 wherein the relatively constant current source comprises a first PMOS transistor, a second PMOS transistor, a first NMOS transistor, a second

NMOS transistor, and a resistor having a first end and a second end, each of the transistors having a gate node, a source node, and a drain node, the drain node of the first PMOS transistor being coupled to the drain node of the first NMOS transistor, the drain node of the second PMOS transistor being coupled to the drain node of the second NMOS transistor, the gate nodes of the first and second PMOS transistors being coupled to the drain node of the first NMOS transistor and to the inverting amplifier, the gate nodes of the first and second NMOS transistors being coupled to the drain node of the second NMOS transistor, the source node of the first NMOS transistor being coupled to the first end of the resistor, and the relatively constant bias voltage being created at the gate nodes of the first and second PMOS transistors.

13. (Currently amended) A real time clock oscillator circuit comprising:

an amplifier having an input ~~for receiving~~ to receive an oscillating signal and an output ~~for generating~~ to generate an amplified oscillating signal, a portion of the amplified oscillating signal being fed back to the input of the amplifier; and

a relatively constant current source having a bias node with a bias voltage that biases the amplifier in an operating state capable of sustained amplification of the oscillating signal, the current source and the amplifier not forming a feedback loop.

14. (Currently amended) The real time clock oscillator circuit of claim 13 wherein the relatively constant current source ~~is configured to generate~~ generates the bias voltage at a level that biases the amplifier to operate at sub-threshold level.

15. (Original) The real time clock oscillator circuit of claim 14 wherein the relatively constant current source also operates at sub-threshold level.

16. (Original) The real time clock oscillator circuit of claim 15 wherein the bias voltage is a direct current voltage that is relatively stable relative to a direct current power supply voltage.

17. (Original) The real time clock oscillator of claim 13 wherein the relatively constant current source comprises a first PMOS transistor, a second PMOS transistor, a first NMOS transistor, a second NMOS transistor, and a resistor having a first end and a second end, each of the transistors having a gate node, a source node, and a drain node, the drain node of the first PMOS transistor being coupled to the drain node of the first NMOS transistor, the drain node of the second PMOS transistor being coupled to the drain node of the second NMOS transistor, the gate nodes of the first and second PMOS transistors being coupled to the drain node of the first NMOS transistor and to the bias node, the gate nodes of the first and second NMOS transistors being coupled to the drain node of the second NMOS transistor, and the source node of the first NMOS transistor being coupled to the first end of the resistor.

18. (Currently amended) Apparatus comprising:

a processor;

a memory ~~adapted~~ to store data;

a chipset ~~for managing~~ to manage data transfers between the memory and the processor; and

a clock oscillator circuit ~~providing~~ to provide time signals during periods when the rest of the apparatus is powered down or powered off, the clock oscillator circuit having

an amplifier for amplifying an oscillating signal, and

a bias circuit having a relatively constant current source ~~for generating~~ to generate a bias voltage at a bias node to bias the amplifier at an operating state that amplifies and sustains the oscillating signal at a low power state, the bias circuit and the amplifier not forming a feedback loop.

19. (Currently amended) The apparatus of claim 18, further comprising a circuit ~~for providing~~ to provide an excitation to the bias circuit, the excitation enabling the bias circuit to provide a stable bias voltage.

20. (Original) The apparatus of claim 18 wherein the clock oscillator circuit includes a plurality of MOSFETs operating in sub-threshold regions.

21. (Original) The apparatus of claim 18 wherein the bias circuit is disposed within an integrated package and is coupled to the amplifier only through the bias node.

22. (Original) The apparatus of claim 18 wherein the relatively constant current source comprises a first PMOS transistor, a second PMOS transistor, a first NMOS transistor, a second NMOS transistor, and a resistor having a first end and a second end, each of the transistors having a gate node, a source node, and a drain node, the drain node of the first PMOS transistor being coupled to the drain node of the first NMOS transistor, the drain node of the second PMOS transistor being coupled to the drain node of the second NMOS transistor, the gate nodes of the first and second PMOS transistors being coupled to the drain node of the first NMOS transistor and to the bias node, the gate nodes of the first and second NMOS transistors being coupled to the drain node of the second NMOS transistor, and the source node of the first NMOS transistor being coupled to the first end of the resistor.

23. (Previously presented) The apparatus of claim 1 in which the inverting amplifier comprises a first P-type transistor and a first N-type transistor and the bias circuit comprises a second P-type transistor and a second N-type transistor, the first P-type transistor having a drain node that is connected to a drain node of the first N-type transistor, the second P-type transistor having a drain node that is connected to a drain node of the second N-type transistor, the first P-type transistor having a gate node that is connected to a gate node of the second P-type transistor, the first P-type transistor and the first N-type transistor having first size ratio, the second P-type transistor and the second N-type transistor having a second size ratio, the first and second size ratios being selected so that the first N-type transistor has a gate-to-source voltage that is slightly higher than a gate-to-source voltage of the second N-type transistor.

24. (Previously presented) The apparatus of claim 23 in which the first and second size ratios are selected so that the gate-to-source voltage of the first N-type transistor is higher than the gate-to-source voltage of the second N-type transistor by an amount sufficient to provide a loop gain that can sustain an oscillation of the oscillator circuit when there are manufacturing tolerances in manufacturing the transistors.

25. (Previously presented) The apparatus of claim 1 in which the inverting amplifier comprises a first P-type transistor and a first N-type transistor and the bias circuit comprises a second P-type transistor and a second N-type transistor, the first P-type transistor having a drain node that is connected to a drain node of the first N-type transistor, the second P-type transistor having a drain node that is connected to a drain node of the second N-type transistor, the first N-type transistor having a gate node that is connected to a gate node of the second N-type transistor, the sizes of the transistors being selected so that the first P-type transistor has a gate-to-source voltage that is similar to and slightly higher than a gate-to-source voltage of the second P-type transistor.

26. (Previously presented) The apparatus of claim 25 in which the first and second size ratios are selected so that the gate-to-source voltage of the first P-type transistor is higher than the gate-to-source voltage of the second P-type transistor by an amount sufficient to provide a loop gain that can sustain an oscillation of the oscillator circuit when there are manufacturing tolerances in manufacturing the transistors.